

CLAIMS

What is claimed is:

1. A computer-implemented method for generating a test program for an integrated circuit design employing a boundary scan implementation, the method comprising:

determining, from a netlist that describes the integrated circuit design, design information including the design architecture and type, name and direction of input and output ports used by the design;

generating a current set of test vectors from the design information;

simulating the operation of the design using the current set of test vectors and storing result data output during the simulation;

generating a new current set of test vectors as a function of the result data;

repeating the steps of simulating, storing result data and generating a new current set of test vectors until selected completion criteria are satisfied; and

in response to the selected completion criteria being satisfied, generating the test program from the result data.

2. The method of claim 1, wherein storing result data includes storing result data indicative of characteristics of the design and the boundary scan implementation and wherein repeating the steps of simulating, storing result data and generating a new current set of test vectors until selected completion criteria are satisfied includes repeating the steps until sufficient characteristics of the design and boundary scan implementation are determined to generate the test program.

3. The method of claim 2, further comprising using the stored result data to determine circuit connectivity in the design and boundary scan implementation and repeating the

steps of simulating, storing result data and using the stored result data to determine circuit connectivity until sufficient circuit connectivity characteristics of the design and boundary scan implementation are determined.

4. The method of claim 3, wherein using the stored result data to determine circuit connectivity includes using the stored result data to map input boundary cells to boundary scan access ports.

5. The method of claim 4, further comprising using the stored result data to map input boundary cells to a particular type of input instruction.

6. The method of claim 3, wherein using the stored result data to determine circuit connectivity includes using the stored result data to map output boundary cells to boundary scan access ports:

7. The method of claim 3, wherein using the stored result data to determine circuit connectivity includes using the stored result data to map control circuits to boundary scan access ports.

8. The method of claim 2, further comprising using the stored result data to determine circuit elements of the design and boundary scan implementation and repeating the steps of simulating, storing result data and using the stored result data to determine circuit elements of the design and boundary scan implementation until sufficient circuit element characteristics of the design and boundary scan implementation are determined.

9. The method of claim 8, wherein using the stored result data to determine circuit elements includes using the stored

result data to map the circuit elements to boundary scan access ports.

10. The method of claim 1, wherein generating a new current set of test vectors includes generating verilog test vectors.

11. The method of claim 1, wherein generating a new set of test vectors includes generating new test vectors that are more comprehensive than the current test vectors.

12. The method of claim 1, further comprising using the result data to identify circuit characteristics of the design and boundary scan implementation, wherein generating a new current set of test vectors includes generating new test vectors that use the identified circuit characteristics.

13. The method of claim 1, wherein generating the test program from the new current set of test vectors includes generating a boundary scan description language (BSDL) file.

14. A method for analyzing an integrated circuit having boundary scan cells, the method comprising:

- determining architecture and I/O pin connectivity of the integrated circuit from a netlist that describes the design of the integrated circuit;

- using the determined architecture and I/O pin connectivity, generating and applying test vectors to a computer-simulated design of the integrated circuit; and

- determining further characteristics of the integrated circuit design and boundary scan cells as a function of a response of the computer-simulated design to the test vectors and, therefrom, generating a test program for analyzing the integrated circuit.

15. For use with an integrated circuit design having test input/output (I/O) ports , a plurality of interconnects

coupled to the test I/O ports and a boundary scan implementation therefor, a testing system comprising:

a test controller programmed to determine, from a netlist that describes the integrated circuit design, design information including the design architecture and type, name and direction of the I/O ports, the test controller further adapted to generate a current set of test vectors from the design information for simulating the operation of the design and the boundary scan implementation;

a storage circuit adapted to store result data output during the simulation, the test controller being further adapted to generate a new current set of test vectors as a function of the result data and to repeat the steps of simulating, storing result data and generating a new current set of test vectors until selected completion criteria are satisfied; and

a test program generator adapted to generate, in response to the selected completion criteria being satisfied, a test program from the result data.

16. The testing system of claim 15, wherein the test controller is a computer programmed to simulate the operation of the integrated circuit design and boundary scan implementation thereof in response to the test vectors.

17. The testing system of claim 15, wherein the integrated circuit design includes a plurality of boundary scan cells coupled to the I/O ports and wherein the test controller is coupled to apply the test vectors to the I/O ports via the boundary scan cells and wherein the storage circuit receives the result data output via the boundary scan cells.

18. The testing system of claim 17, wherein the storage circuit is adapted to store result data output during the simulation that is indicative of the connectivity of the boundary scan cells to the I/O ports and to generate the new

current set of test vectors as a function of the indicated connectivity of the boundary scan cells to the I/O ports.

19. The testing system of claim 17, wherein the integrated circuit design includes at least two distinct circuits, each distinct circuit having test I/O ports and associated boundary scan cells coupled thereto, the plurality of boundary scan cells being coupled in a chain with output boundary scan cells from a first one of the at least two distinct circuits being coupled to input boundary scan cells of a second one of the at least two distinct circuits, wherein the storage circuit is adapted to store result data indicative of the chain connectivity of the output boundary scan cells to the input boundary scan cells and wherein the test program generator is adapted to generate the test program as a function of the chain connectivity.

20. A boundary scan description language (BSDL) file generator comprising:

- a netlister tool adapted to netlist a circuit design having a boundary scan implementation;

- a test vector generator adapted to parse a circuit design netlisted by the netlister tool to determine the type, name and direction of ports used by the design and to generate an initial set of test vectors;

- an analyzer adapted to analyze outputs of the circuit design in response to the test vectors and to determine characteristics of the circuit design and the boundary scan implementation;

- the test vector generator being further adapted to use the determined characteristics to generate new comprehensive test vectors, the analyzer being further adapted to analyze outputs of the circuit design in response to the new comprehensive test vectors; and

- a program generator adapted to use the analyzed outputs to generate the BSDL file for the circuit design.